

# ABSTRACT OF THE INVENTION

A semiconductor integrated circuit testing system for testing electric characteristics of a plurality of semiconductor integrated circuit devices formed on a semiconductor wafer in the lump includes a wafer tray for holding the semiconductor wafer and an interconnect substrate facing the semiconductor wafer held on the wafer tray and having interconnect layers to which a testing voltage is externally input. A ring-shaped sealing member is provided between the wafer tray and the interconnect substrate so as to form a sealed space together with the wafer tray and the interconnect substrate. An elastic sheet is held on the interconnect substrate at the periphery thereof. A plurality of probe terminals electrically connected to the interconnect layers are provided on the elastic sheet in positions respectively corresponding to external electrodes of the plural semiconductor integrated circuit devices. A plurality of protrusions protruding toward the wafer tray are provided on the elastic sheet for preventing the interconnect substrate from deforming toward the wafer tray when the internal pressure of the sealed space is reduced.